10-Bit, 20/40/60MSPS A/D Converter with Internal Voltage Reference

The HI5767 is a monolithic, 10-bit, analog-to-digital converter fabricated in a CMOS process. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its high sample clock rate is made possible by a fully differential pipelined architecture with both an internal sample and hold and internal band-gap voltage reference.

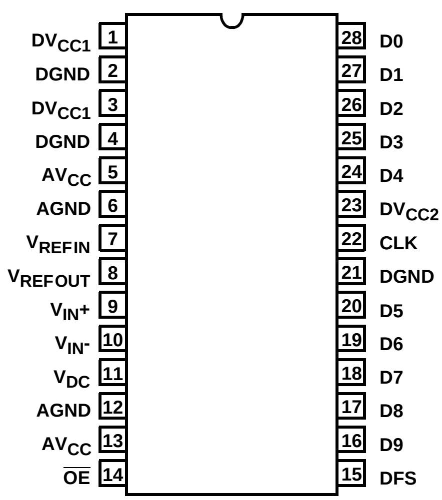
The 250MHz Full Power Input Bandwidth and superior high frequency performance of the HI5767 converter make it an excellent choice for implementing Digital IF architectures in communications applications.

The HI5767 has excellent dynamic performance while consuming only 310mW power at 40MSPS. Data output latches are provided which present valid data to the output bus with a latency of 7 clock cycles.

The HI5767 is offered in 20MSPS, 40MSPS and 60MSPS sampling rates.

Pinout

HI5767 (SOIC, SSOP)
TOP VIEW



Features

- Sampling Rate 20/40/60MSPS
- 8.8 Bits at f_{IN} = 10MHz, f_S = 40MSPS
- Low Power at 40MSPS 310mW
- Wide Full Power Input Bandwidth 250MHz
- On-Chip Sample and Hold
- Internal 2.5V Band-Gap Voltage Reference
- Fully Differential or Single-Ended Analog Input
- Single Supply Voltage . . . .+5V
- TTL/CMOS Compatible Digital Inputs
- CMOS Compatible Digital Outputs. 3.0V/5.0V
- Offset Binary or Two's Complement Output Format
- Pb-Free Available (RoHS Compliant)

Applications

- Digital Communication Systems
- QAM Demodulators
- Professional Video Digitizing
- Medical Imaging
- High Speed Data Acquisition

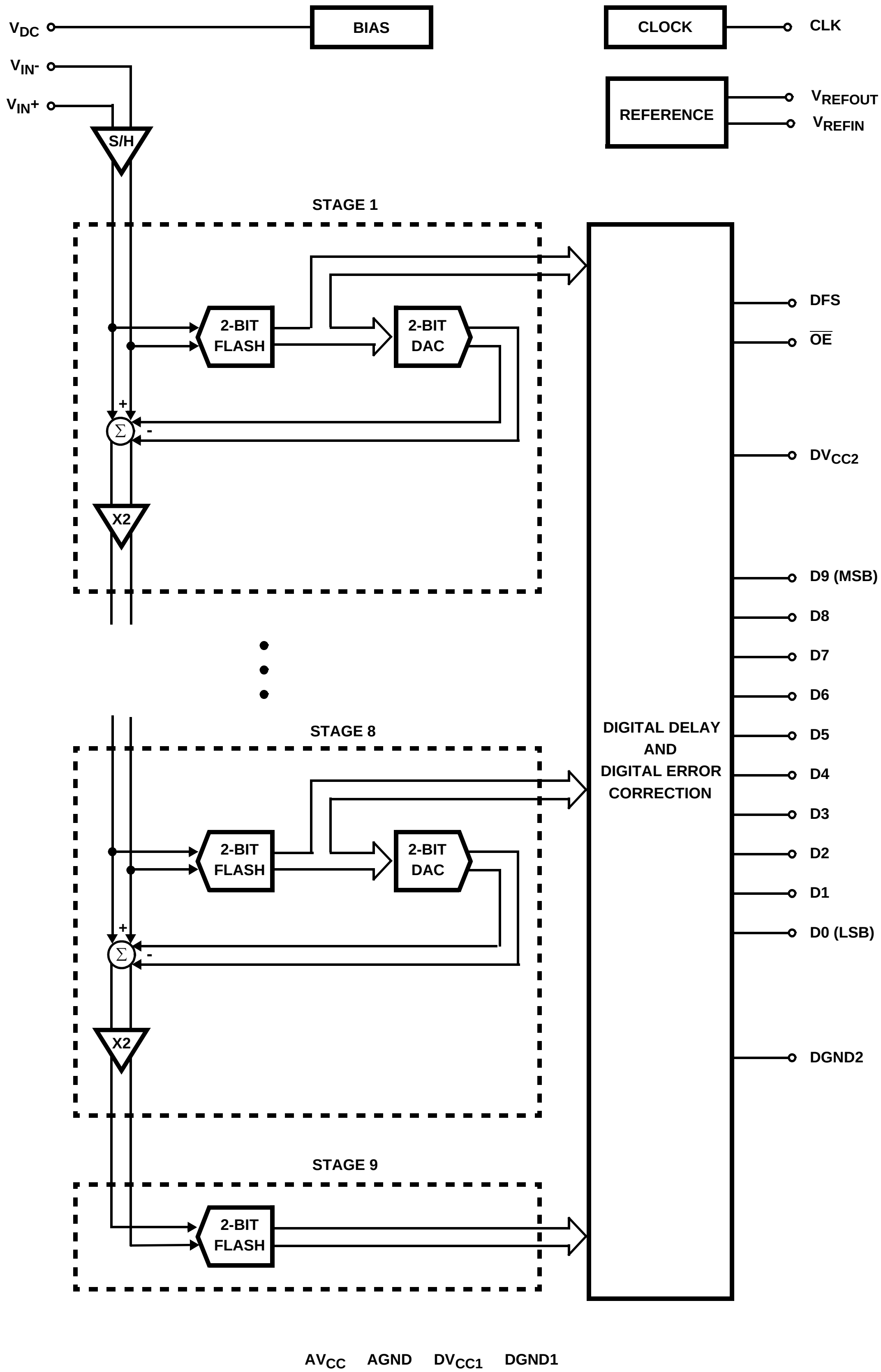
Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. DWG. #	SAMPLING RATE (MSPS)
HI5767/2CB	0 to 70	28 Ld SOIC	M28.3	20
HI5767/2CBZ (See Note)	0 to 70	28 Ld SOIC (Pb-free)	M28.3	20
HI5767/4CB*	0 to 70	28 Ld SOIC	M28.3	40
HI5767/4CBZ* (See Note)	0 to 70	28 Ld SOIC (Pb-free)	M28.3	40
HI5767/6CB*	0 to 70	28 Ld SOIC	M28.3	60
HI5767/6CBZ* (See Note)	0 to 70	28 Ld SOIC (Pb-free)	M28.3	60
HI5767/6IB	-40 to 85	28 Ld SOIC	M28.3	60
HI5767/6IBZ (See Note)	-40 to 85	28 Ld SOIC (Pb-free)	M28.3	60
HI5767/2CA	0 to 70	28 Ld SSOP	M28.15	20
HI5767/2CAZ (See Note)	0 to 70	28 Ld SSOP (Pb-free)	M28.15	20
HI5767/2IA	-40 to 85	28 Ld SSOP	M28.15	20
HI5767/2IAZ (See Note)	-40 to 85	28 Ld SSOP (Pb-free)	M28.15	20
HI5767/4CA	0 to 70	28 Ld SSOP	M28.15	40
HI5767/4CAZ (See Note)	0 to 70	28 Ld SSOP (Pb-free)	M28.15	40
HI5767/6CA	0 to 70	28 Ld SSOP	M28.15	60
HI5767/6CAZ (See Note)	0 to 70	28 Ld SSOP (Pb-free)	M28.15	60
HI5767EVAL1	25	Evaluation Board		60
HI5767EVAL2	25	Evaluation Board		60

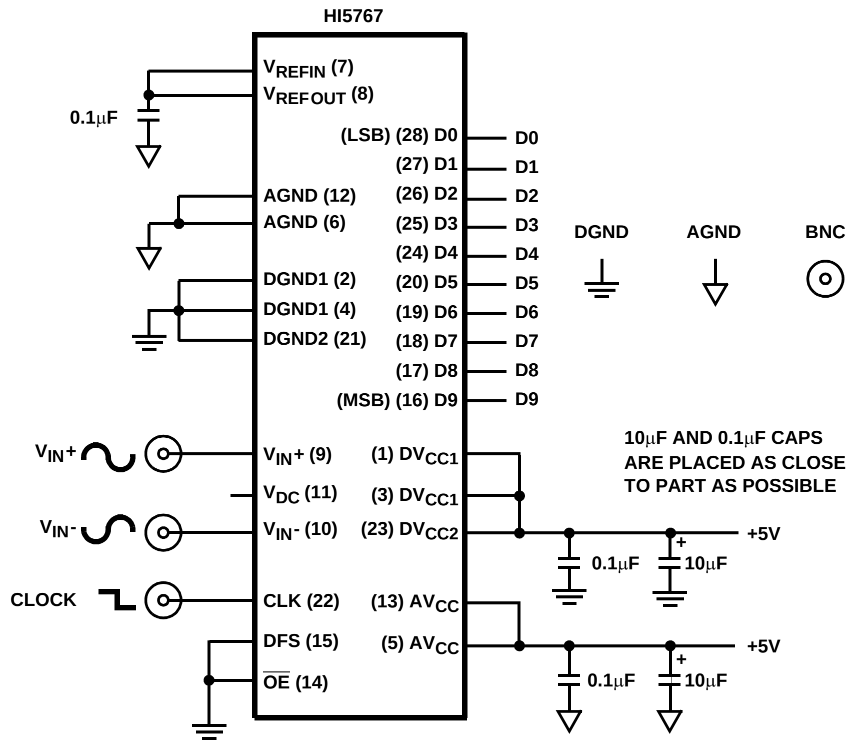
* Add “-T” suffix for tape and reel.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Functional Block Diagram



Typical Application Schematic



Pin Descriptions

PIN NO.	NAME	DESCRIPTION
1	DV_{CC1}	Digital Supply (+5.0V)
2	DGND1	Digital Ground
3	DV_{CC1}	Digital Supply (+5.0V)
4	DGND1	Digital Ground
5	AV_{CC}	Analog Supply (+5.0V)
6	AGND	Analog Ground
7	V_{REFIN}	+2.5V Reference Voltage Input
8	V_{REFOUT}	+2.5V Reference Voltage Output
9	$V_{IN}+$	Positive Analog Input
10	$V_{IN}-$	Negative Analog Input
11	V_{DC}	DC Bias Voltage Output
12	AGND	Analog Ground
13	AV_{CC}	Analog Supply (+5.0V)
14	$\overline{OE}$	Digital Output Enable Control Input

PIN NO.	NAME	DESCRIPTION
15	DFS	Data Format Select Input
16	D9	Data Bit 9 Output (MSB)
17	D8	Data Bit 8 Output
18	D7	Data Bit 7 Output
19	D6	Data Bit 6 Output
20	D5	Data Bit 5 Output
21	DGND2	Digital Ground
22	CLK	Sample Clock Input
23	DV_{CC2}	Digital Output Supply (+3.0V or +5.0V)
24	D4	Data Bit 4 Output
25	D3	Data Bit 3 Output
26	D2	Data Bit 2 Output
27	D1	Data Bit 1 Output
28	D0	Data Bit 0 Output (LSB)

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage, AV_{CC} or DV_{CC} to AGND or DGND 6V
DGND to AGND 0.3V
Digital I/O Pins . . . . DGND to DV_{CC}
Analog I/O Pins . . . . AGND to AV_{CC}

Operating Conditions

Temperature Range
HI5767/xCx. . . . . 0^oC to 70^oC
HI5767/xIx . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	75
SSOP Package	100

Maximum Junction Temperature . . . . 150^oC
Maximum Storage Temperature Range . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$AV_{CC} = DV_{CC1} = 5.0V$, $DV_{CC2} = 3.0V$; $V_{REFIN} = V_{REFOUT}$; $f_S = 40MSPS$ at 50% Duty Cycle; $C_L = 10pF$; $T_A = 25^oC$; Differential Analog Input; Typical Values are Test Results at 25^oC, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	f_{IN} = 1MHz Sinewave	-	±0.75	±1.75	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_{IN} = 1MHz Sinewave	-	±0.35	±1.0	LSB
Offset Error, V_{OS}	f_{IN} = DC	-40	-	40	LSB
Full Scale Error, FSE	f_{IN} = DC	-	4	-	LSB
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes	-	0.5	1	MSPS
Maximum Conversion Rate					
HI5767/2	No Missing Codes	20	-	-	MSPS
HI5767/4	No Missing Codes	40	-	-	MSPS
HI5767/6	No Missing Codes	60	-	-	MSPS
Effective Number of Bits, ENOB					
HI5767/2	f_S = 20MSPS, f_{IN} = 10MHz	8.7	9	-	Bits
HI5767/4	f_S = 40MSPS, f_{IN} = 10MHz	8.55	8.8	-	Bits
HI5767/6	f_S = 60MSPS, f_{IN} = 10MHz	8.1	8.4	-	Bits
Signal to Noise and Distortion Ratio, SINAD $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$					
HI5767/2	f_S = 20MSPS, f_{IN} = 10MHz	-	55.9	-	dB
HI5767/4	f_S = 40MSPS, f_{IN} = 10MHz	-	54.7	-	dB
HI5767/6	f_S = 60MSPS, f_{IN} = 10MHz	-	53.8	-	dB
Signal to Noise Ratio, SNR $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$					
HI5767/2	f_S = 20MSPS, f_{IN} = 10MHz	-	55.9	-	dB
HI5767/4	f_S = 40MSPS, f_{IN} = 10MHz	-	55	-	dB
HI5767/6	f_S = 60MSPS, f_{IN} = 10MHz	-	54	-	dB
Total Harmonic Distortion, THD					
HI5767/2	f_S = 20MSPS, f_{IN} = 10MHz	-	-71	-	dBc

Electrical Specifications

$AV_{CC} = DV_{CC1} = 5.0V$, $DV_{CC2} = 3.0V$; $V_{REFIN} = V_{REFOUT}$; f_S = 40MSPS at 50% Duty Cycle; C_L = 10pF; $T_A = 25^oC$; Differential Analog Input; Typical Values are Test Results at 25^oC, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
HI5767/4	f_S = 40MSPS, f_{IN} = 10MHz	-	-65	-	dBc
HI5767/6	f_S = 60MSPS, f_{IN} = 10MHz	-	-64.5	-	dBc
2nd Harmonic Distortion					
HI5767/2	f_S = 20MSPS, f_{IN} = 10MHz	-	-76	-	dBc
HI5767/4	f_S = 40MSPS, f_{IN} = 10MHz	-	-73	-	dBc
HI5767/6	f_S = 60MSPS, f_{IN} = 10MHz	-	-70	-	dBc
3rd Harmonic Distortion					
HI5767/2	f_S = 20MSPS, f_{IN} = 10MHz	-	-80	-	dBc
HI5767/4	f_S = 40MSPS, f_{IN} = 10MHz	-	-69	-	dBc
HI5767/6	f_S = 60MSPS, f_{IN} = 10MHz	-	-67	-	dBc
Spurious Free Dynamic Range, SFDR					
HI5767/2	f_S = 20MSPS, f_{IN} = 10MHz	-	76	-	dBc
HI5767/4	f_S = 40MSPS, f_{IN} = 10MHz	-	69	-	dBc
HI5767/6	f_S = 60MSPS, f_{IN} = 10MHz	-	67	-	dBc
Intermodulation Distortion, IMD	f_1 = 1MHz, f_2 = 1.02MHz	-	64	-	dBc
Differential Gain Error	f_S = 17.72MHz, 6 Step, Mod Ramp	-	0.5	-	%
Differential Phase Error	f_S = 17.72MHz, 6 Step, Mod Ramp	-	0.2	-	Degree
Transient Response	(Note 2)	-	1	-	Cycle
Over-Voltage Recovery	0.2V Overdrive (Note 2)	-	1	-	Cycle
ANALOG INPUT					
Maximum Peak-to-Peak Differential Analog Input Range (V_{IN}+ - V_{IN}-)		-	±0.5	-	V
Maximum Peak-to-Peak Single-Ended Analog Input Range		-	1.0	-	V
Analog Input Resistance, R_{IN}	(Note 3)	-	1	-	MΩ
Analog Input Capacitance, C_{IN}		-	10	-	pF
Analog Input Bias Current, I_B+ or I_B-	(Note 3)	-10	-	+10	μA
Differential Analog Input Bias Current I_{BDIFF} = (I_B+ - I_B-)	(Note 3)	-	±0.5	-	μA
Full Power Input Bandwidth, FPBW		-	250	-	MHz
Analog Input Common Mode Voltage Range (V_{IN}+ + V_{IN}-) / 2	Differential Mode (Note 2)	0.25	-	4.75	V
INTERNAL REFERENCE VOLTAGE					
Reference Voltage Output, V_{REFOUT} (Loaded)		-	2.5	-	V
Reference Output Current, I_{REFOUT}		-	1	2	mA
Reference Temperature Coefficient		-	120	-	ppm/^oC
REFERENCE VOLTAGE INPUT					
Reference Voltage Input, V_{REFIN}		-	2.5	-	V
Total Reference Resistance, R_{REFIN}		-	2.5	-	kΩ
Reference Input Current, I_{REFIN}		-	1	-	mA
DC BIAS VOLTAGE					
DC Bias Voltage Output, V_{DC}		-	3.0	-	V

Electrical Specifications

$AV_{CC} = DV_{CC1} = 5.0V$, $DV_{CC2} = 3.0V$; $V_{REFIN} = V_{REFOUT}$; f_S = 40MSPS at 50% Duty Cycle; C_L = 10pF; $T_A = 25^oC$; Differential Analog Input; Typical Values are Test Results at 25^oC, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Output Current		-	-	0.2	mA
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}	CLK, DFS, $\overline{OE}$	2.0	-	-	V
Input Logic Low Voltage, V_{IL}	CLK, DFS, $\overline{OE}$	-	-	0.8	V
Input Logic High Current, I_{IH}	CLK, DFS, $\overline{OE}$, V_{IH} = 5V	-10.0	-	+10.0	μA
Input Logic Low Current, I_{IL}	CLK, DFS, $\overline{OE}$, V_{IL} = 0V	-10.0	-	+10.0	μA
Input Capacitance, C_{IN}		-	7	-	pF
DIGITAL OUTPUTS					
Output Logic High Voltage, V_{OH}	I_{OH} = 100μA; DV_{CC2} = 5V	4.0	-	-	V
Output Logic Low Voltage, V_{OL}	I_{OL} = 100μA; DV_{CC2} = 5V	-	-	0.8	V
Output Three-State Leakage Current, I_{OZ}	V_O = 0/5V; DV_{CC2} = 5V	-10	±1	10	μA
Output Logic High Voltage, V_{OH}	I_{OH} = 100μA; DV_{CC2} = 3V	2.4	-	-	V
Output Logic Low Voltage, V_{OL}	I_{OL} = 100μA; DV_{CC2} = 3V	-	-	0.5	V
Output Three-State Leakage Current, I_{OZ}	V_O = 0/5V; DV_{CC2} = 3V	-10	±1	10	μA
Output Capacitance, C_{OUT}		-	10	-	pF
TIMING CHARACTERISTICS					
Aperture Delay, t_{AP}		-	5	-	ns
Aperture Jitter, t_{AJ}		-	5	-	ps_{RMS}
Data Output Hold, t_H		-	5	-	ns
Data Output Delay, t_{OD}		-	6	-	ns
Data Output Enable Time, t_{EN}		-	5	-	ns
Data Output Enable Time, t_{DIS}		-	5	-	ns
Data Latency, t_{LAT}	For a Valid Sample (Note 2)	-	-	7	Cycles
Power-Up Initialization	Data Invalid Time (Note 2)	-	-	20	Cycles
Sample Clock Pulse Width (Low)	f_S = 40MSPS	11.3	12.5	-	ns
Sample Clock Pulse Width (High)	f_S = 40MSPS	11.3	12.5	-	ns
Sample Clock Duty Cycle Variation	f_S = 40MSPS	-	±5	-	%
POWER SUPPLY CHARACTERISTICS					
Analog Supply Voltage, AV_{CC}		4.75	5.0	5.25	V
Digital Supply Voltage, DV_{CC1}		4.75	5.0	5.25	V
Digital Output Supply Voltage, DV_{CC2}	At 3.0V	2.7	3.0	3.3	V
	At 5.0V	4.75	5.0	5.25	V
Supply Current, I_{CC}	f_{IN} = 1MHz and DFS = “0”	-	62	-	mA
Power Dissipation	f_{IN} = 1MHz and DFS = “0”	-	310	-	mW
Offset Error Sensitivity, ΔV_{OS}	AV_{CC} or DV_{CC} = 5V ±5%	-	±0.7	-	LSB
Gain Error Sensitivity, ΔFSE	AV_{CC} or DV_{CC} = 5V ±5%	-	±0.1	-	LSB

NOTES:

2. Parameter guaranteed by design or characterization and not production tested.
3. With the clock low and DC input.

Timing Waveforms

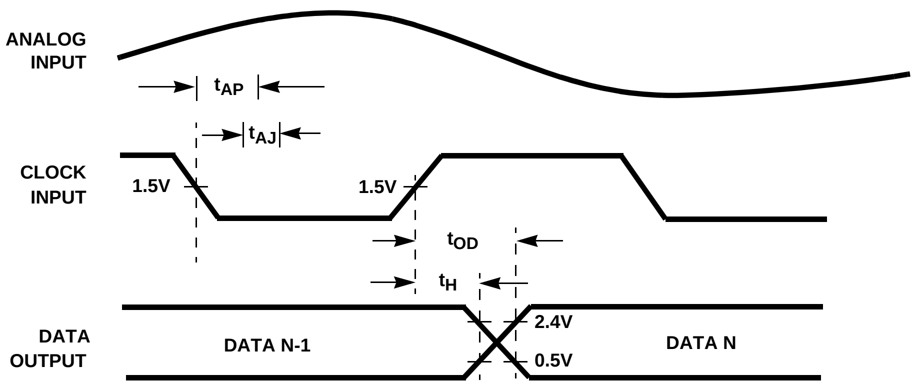


FIGURE 1. INPUT TO OUTPUT TIMING

Typical Performance Curves

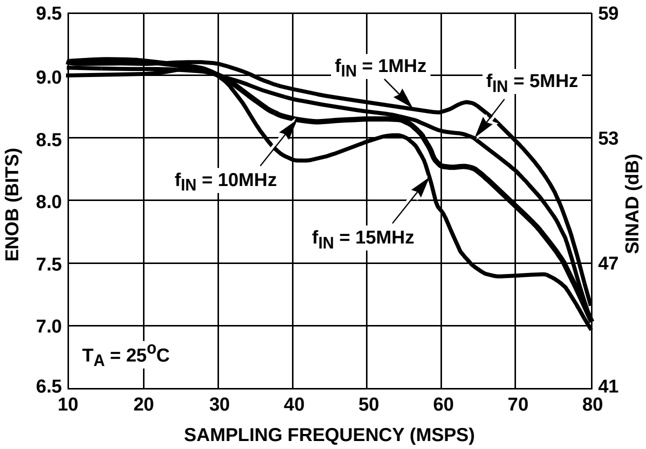


FIGURE 2. EFFECTIVE NUMBER OF BITS (ENOB) AND SINAD vs SAMPLING FREQUENCY

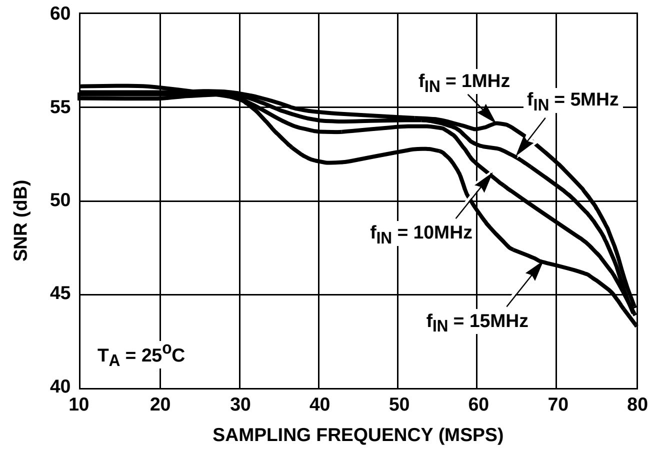


FIGURE 3. SNR vs SAMPLING FREQUENCY

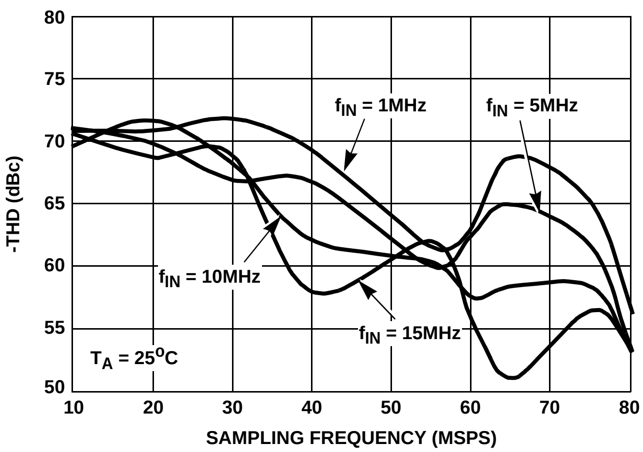


FIGURE 4. -THD vs SAMPLING FREQUENCY

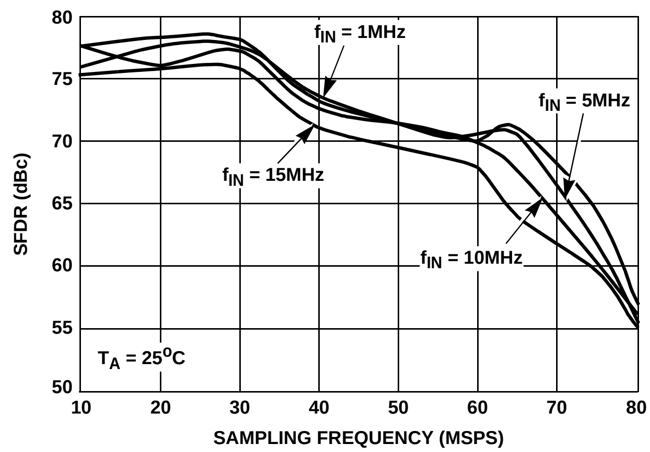


FIGURE 5. SFDR vs SAMPLING FREQUENCY

Typical Performance Curves (Continued)

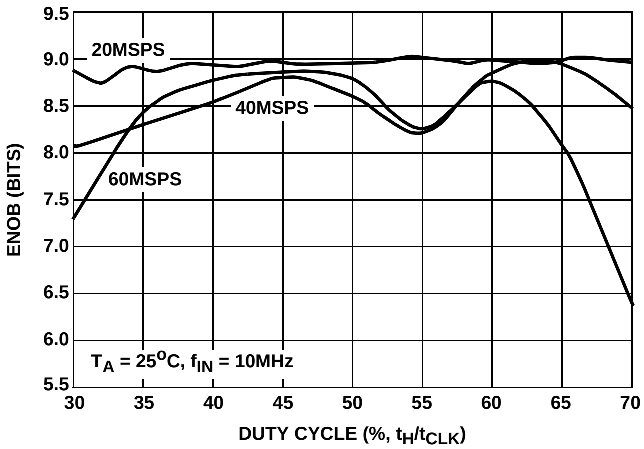


FIGURE 6. EFFECTIVE NUMBER OF BITS (ENOB) vs SAMPLE CLOCK DUTY CYCLE

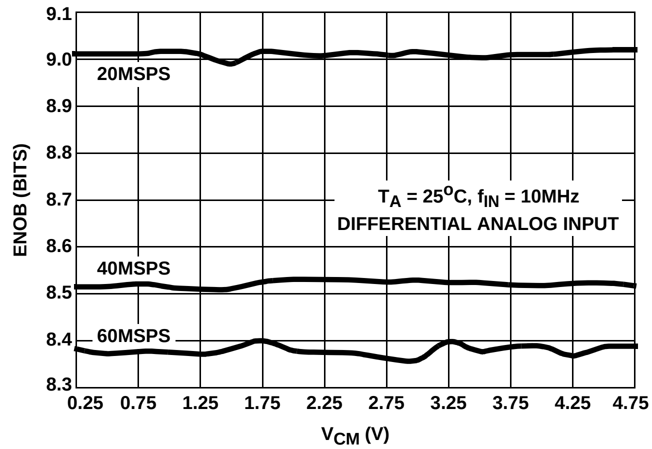


FIGURE 7. EFFECTIVE NUMBER OF BITS (ENOB) vs ANALOG INPUT COMMON MODE VOLTAGE

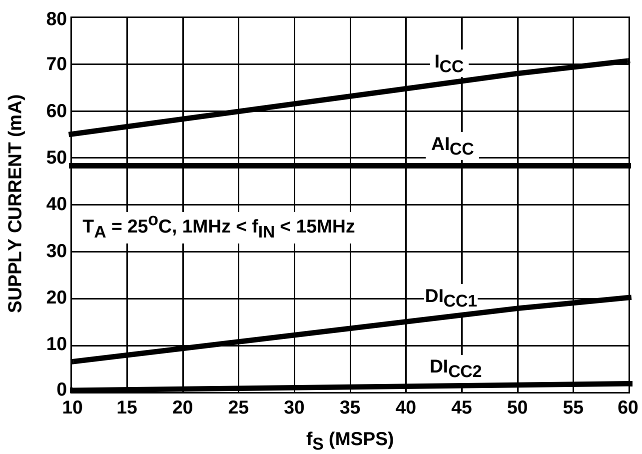


FIGURE 8. SUPPLY CURRENT vs SAMPLE CLOCK FREQUENCY

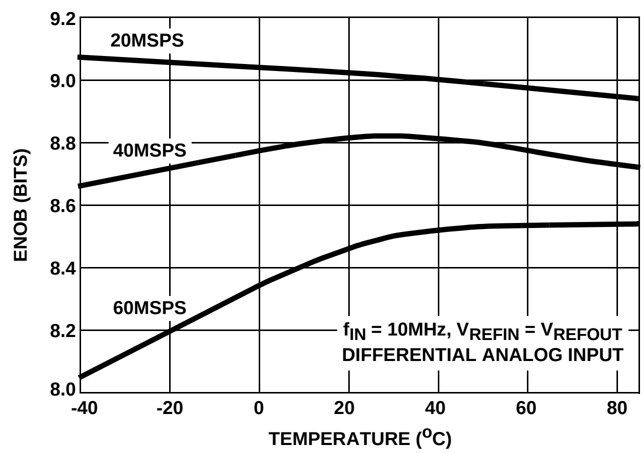


FIGURE 9. EFFECTIVE NUMBER OF BITS (ENOB) vs TEMPERATURE

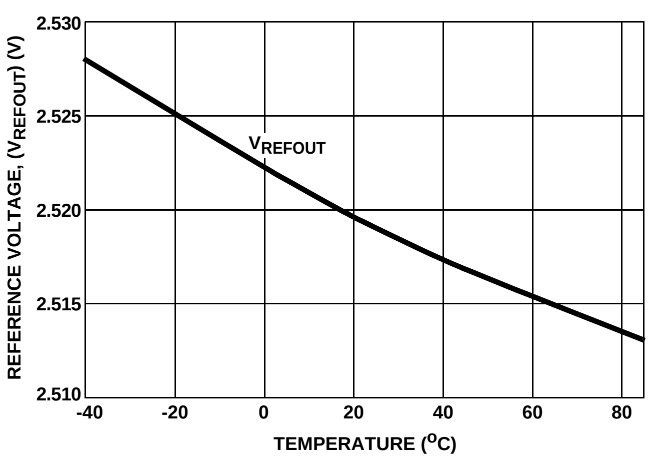


FIGURE 10. INTERNAL REFERENCE VOLTAGE (V_{REFOUT}) vs TEMPERATURE

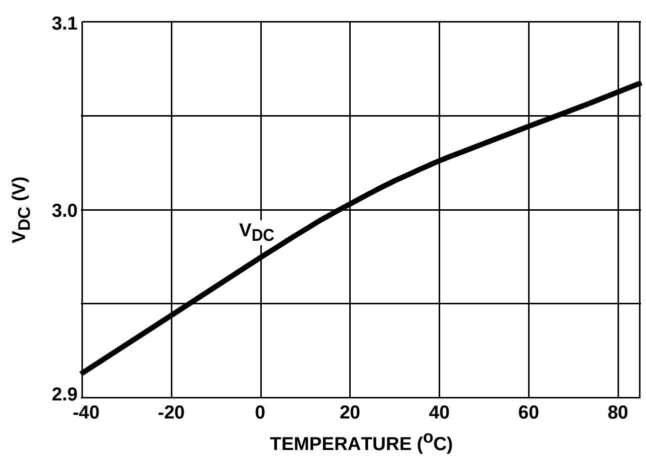


FIGURE 11. DC BIAS VOLTAGE (V_{DC}) vs TEMPERATURE

Typical Performance Curves (Continued)

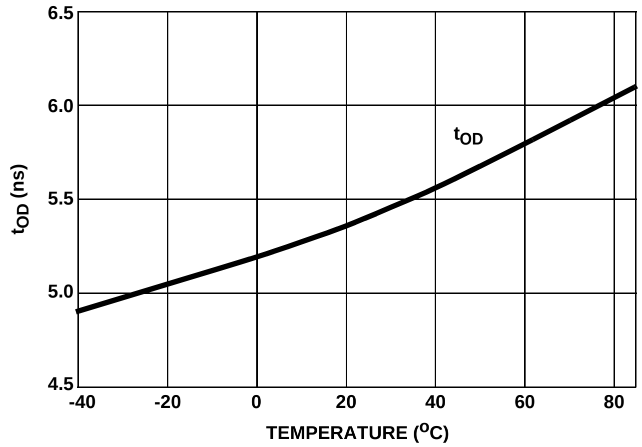


FIGURE 12. DATA OUTPUT DELAY (t_{OD}) vs TEMPERATURE

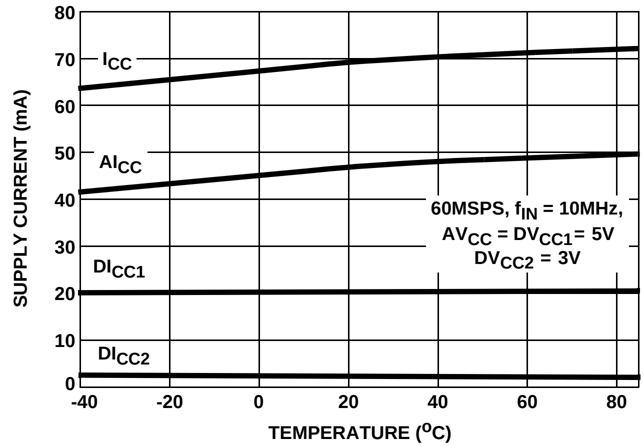


FIGURE 13. SUPPLY CURRENT vs TEMPERATURE

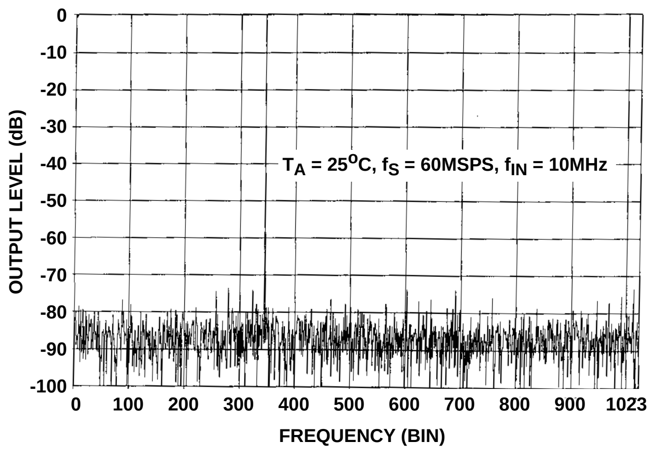


FIGURE 14. 2048 POINT FFT PLOT

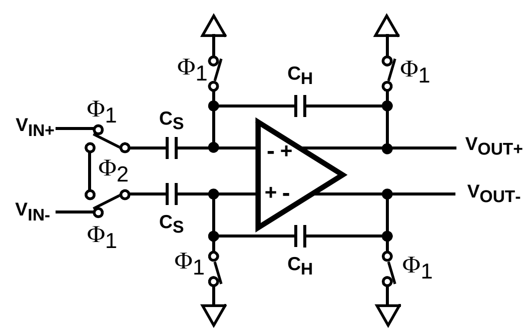


FIGURE 15. ANALOG INPUT SAMPLE-AND-HOLD

TABLE 1. A/D CODE TABLE

CODE CENTER DESCRIPTION	DIFFERENTIAL INPUT VOLTAGE ($V_{IN}+ - V_{IN}-$)	OFFSET BINARY OUTPUT CODE (DFS LOW)										TWO'S COMPLEMENT OUTPUT CODE (DFS HIGH)									
		MSB									LSB	MSB									LSB
		D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
+Full Scale (+FS) - $^{1}/_{4}$ LSB	0.499756V	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
+FS - $1^{1}/_{4}$ LSB	0.498779V	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0
+$^{3}/_{4}$ LSB	732.422µV	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-$^{1}/_{4}$ LSB	-244.141µV	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
-FS + $1^{3}/_{4}$ LSB	-0.498291V	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1
-Full Scale (-FS) + $^{3}/_{4}$ LSB	-0.499268V	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

NOTE:

4. The voltages listed above represent the ideal center of each output code shown with V_{REFIN} = +2.5V.

Detailed Description

Theory of Operation

The HI5767 is a 10-bit fully differential sampling pipeline A/D converter with digital error correction logic. Figure 16 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal sampling clock which is a non-overlapping two phase signal, Φ_1 and Φ_2, derived from the master sampling clock. During the sampling phase, Φ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of Φ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, Φ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op-amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The front end sample-and-hold output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of a switch and C_S. The relatively small values of these components result in a typical full power input bandwidth of 250MHz for the converter.

As illustrated in the functional block diagram and the timing diagram in Figure 1, eight identical pipeline subconverter stages, each containing a two-bit flash converter and a two-bit multiplying digital-to-analog converter, follow the S/H circuit with the ninth stage being a two bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual subconverter clock signal is offset by 180 degrees from the previous stage clock signal resulting in alternate stages in the pipeline performing the same operation.

The output of each of the eight identical two-bit subconverter stages is a two-bit digital word containing a supplementary bit to be used by the digital error correction logic. The output of each subconverter stage is input to a digital delay line which is controlled by the internal sampling clock. The function of the digital delay line is to time align the digital outputs of the eight identical two-bit subconverter stages with the corresponding output of the ninth stage flash converter before applying the eighteen bit result to the digital error correction logic. The digital error correction logic uses the supplementary bits to correct any error that may exist before generating the final ten bit digital data output of the converter.

Because of the pipeline nature of this converter, the digital data representing an analog input sample is output to the digital data bus on the 7th cycle of the clock after the analog sample is taken. This time delay is specified as the data latency. After the data latency time, the digital data representing each succeeding analog sample is output during the following clock cycle. The digital output data is synchronized to the external sampling clock by a double buffered latching technique. The digital output data is available in two's complement or offset binary format depending on the state of the Data Format Select (DFS) control input (see Table 1, A/D Code Table).

Internal Reference Voltage Output, V_{REFOUT}

The HI5767 is equipped with an internal reference voltage generator, therefore, no external reference voltage is required. V_{REFOUT} must be connected to V_{REFIN} when using the internal reference voltage.

An internal band-gap reference voltage followed by an amplifier/buffer generates the precision +2.5V reference voltage used by the converter. A 4:1 array of substrate PNPs generates the "delta-V_{BE}" and a two-stage op-amp closes the loop to create an internal +1.25V band-gap reference voltage. This voltage is then amplified by a wideband uncompensated operational amplifier connected in a gain-of-two configuration. An external, user-supplied, 0.1μF capacitor connected from the V_{REFOUT} output pin to analog ground is used to set the dominant pole and to maintain the stability of the operational amplifier.

Reference Voltage Input, V_{REFIN}

The HI5767 is designed to accept a +2.5V reference voltage source at the V_{REFIN} input pin. Typical operation of the converter requires V_{REFIN} to be set at +2.5V. The HI5767 is tested with V_{REFIN} connected to V_{REFOUT} yielding a fully differential analog input voltage range of ±0.5V.

The user does have the option of supplying an external +2.5V reference voltage. As a result of the high input impedance presented at the V_{REFIN} input pin, 2.5kΩ typically, the external reference voltage being used is only required to source 1mA of reference input current. In the situation where an external reference voltage will be used an external 0.1μF capacitor **must** be connected from the V_{REFOUT} output pin to analog ground in order to maintain the stability of the internal operational amplifier.

In order to minimize overall converter noise it is recommended that adequate high frequency decoupling be provided at the reference voltage input pin, V_{REFIN}.

Analog Input, Differential Connection

The analog input to the HI5767 is a differential input that can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (Figure 17 and Figure 18) will deliver the best performance from the converter.

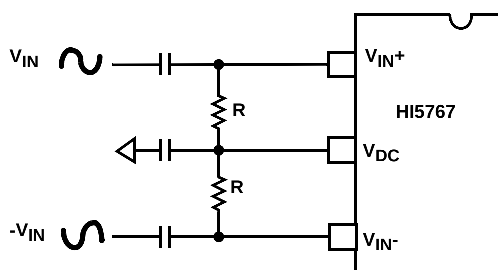


FIGURE 16. AC COUPLED DIFFERENTIAL INPUT

Since the HI5767 is powered by a single +5V analog supply, the analog input is limited to be between ground and +5V. For the differential input connection this implies the analog input common mode voltage can range from 0.25V to 4.75V. The performance of the ADC does not change significantly with the value of the analog input common mode voltage.

A DC voltage source, V_{DC}, equal to 3.2V (typical), is made available to the user to help simplify circuit design when using an AC coupled differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent DC bias source and stays well within the analog input common mode voltage range over temperature.

For the AC coupled differential input (Figure 17) and with V_{REFIN} connected to V_{REFOUT}, full scale is achieved when the V_{IN} and $-V_{IN}$ input signals are $0.5V_{P-P}$, with $-V_{IN}$ being 180 degrees out of phase with V_{IN}. The converter will be at positive full scale when the $V_{IN}+$ input is at V_{DC} + 0.25V and the $V_{IN}-$ input is at V_{DC} - 0.25V ($V_{IN}+ - V_{IN}- = +0.5V$). Conversely, the converter will be at negative full scale when the $V_{IN}+$ input is equal to V_{DC} - 0.25V and $V_{IN}-$ is at V_{DC} + 0.25V ($V_{IN}+ - V_{IN}- = -0.5V$).

The analog input can be DC coupled (Figure 18) as long as the inputs are within the analog input common mode voltage range (0.25V ≤ VDC ≤ 4.75V).

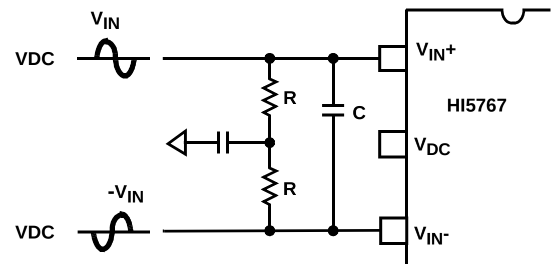


FIGURE 17. DC COUPLED DIFFERENTIAL INPUT

The resistors, R, in Figure 18 are not absolutely necessary but may be used as load setting resistors. A capacitor, C, connected from $V_{IN}+$ to $V_{IN}-$ will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

Analog Input, Single-Ended Connection

The configuration shown in Figure 19 may be used with a single ended AC coupled input.

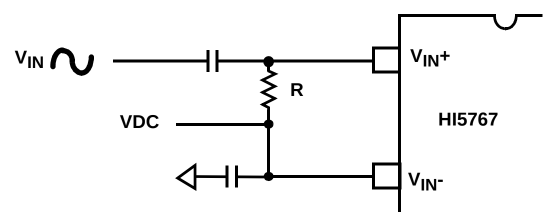


FIGURE 18. AC COUPLED SINGLE ENDED INPUT

Again, with V_{REFIN} connected to V_{REFOUT}, if V_{IN} is a $1V_{P-P}$ sinewave, then $V_{IN}+$ is a $1.0V_{P-P}$ sinewave riding on a positive voltage equal to VDC. The converter will be at positive full scale when $V_{IN}+$ is at VDC + 0.5V ($V_{IN}+ - V_{IN}- = +0.5V$) and will be at negative full scale when $V_{IN}+$ is equal to VDC - 0.5V ($V_{IN}+ - V_{IN}- = -0.5V$). Sufficient headroom must be provided such that the input voltage never goes above +5V or below AGND. In this case, VDC could range between 0.5V and 4.5V without a significant change in ADC performance. The simplest way to produce VDC is to use the DC bias source, V_{DC}, output of the HI5767.

The single ended analog input can be DC coupled (Figure 20) as long as the input is within the analog input common mode voltage range.

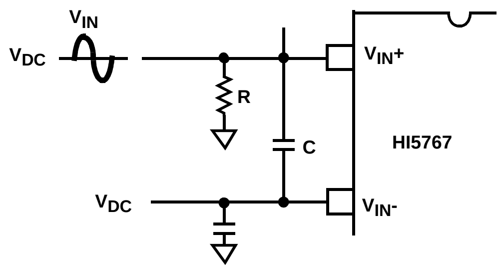


FIGURE 19. DC COUPLED SINGLE ENDED INPUT

The resistor, R, in Figure 20 is not absolutely necessary but may be used as a load setting resistor. A capacitor, C, connected from $V_{IN}+$ to $V_{IN}-$ will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

A single ended source may give better overall system performance if it is first converted to differential before driving the HI5767.

Digital Output Control and Clock Requirements

The HI5767 provides a standard high-speed interface to external TTL logic families.

In order to ensure rated performance of the HI5767, the duty cycle of the clock should be held at 50% $\pm$5%. It must also have low jitter and operate at standard TTL levels.

Performance of the HI5767 will only be guaranteed at conversion rates above 1 MSPS. This ensures proper performance of the internal dynamic circuits. Similarly, when power is first applied to the converter, a maximum of 20 cycles at a sample rate above 1 MSPS will have to be performed before valid data is available.A Data Format Select (DFS) pin is provided which will determine the format of the digital data outputs. When at logic low, the data will be output in offset binary format. When at logic high, the data will be output in two's complement format. Refer to Table 1 for further information.

The output enable pin, $\overline{OE}$, when pulled high will three-state the digital outputs to a high impedance state. Set the $\overline{OE}$ input to logic low for normal operation.

$\overline{OE}$ INPUT	DIGITAL DATA OUTPUTS
0	Active
1	High Impedance

Supply and Ground Considerations

The HI5767 has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The digital data outputs also have a separate supply pin, DV_{CC2}, which can be powered from a 3.0V or 5.0V supply. This allows the outputs to interface with 3.0V logic if so desired.

The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds. For best performance, the supplies to the HI5767 should be driven by clean, linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the converter. If the part is powered off a single supply, then the analog supply should be isolated with a ferrite bead from the digital supply.

Refer to the application note "Using Intersil High Speed A/D Converters" (AN9214) for additional considerations when using high speed converters.

Static Performance Definitions

Offset Error (V_{OS})

The midscale code transition should occur at a level $^1/_4$ LSB above half-scale. Offset is defined as the deviation of the actual code transition from this point.

Full-Scale Error (FSE)

The last code transition should occur for an analog input that is $^3/_4$ LSB below Positive Full Scale (+FS) with the offset error removed. Full scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Sensitivity

Each of the power supplies are moved plus and minus 5% and the shift in the offset and full scale error (in LSBs) is noted.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5767. A low distortion sine wave is applied to the input, it is coherently sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with an FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is typically -0.5dB down from full scale for all these tests.

SNR and SINAD are quoted in dB. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

The Effective Number of Bits (ENOB) is calculated from the SINAD data by:

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02,$$

where: V_{CORR} = 0.5 dB (Typical).

V_{CORR} adjusts the SINAD, and hence the ENOB, for the amount the analog input signal is backed off from full scale.

Signal To Noise and Distortion Ratio (SINAD)

SINAD is the ratio of the measured RMS signal to RMS sum of all the other spectral components below the Nyquist frequency, $f_S/2$, excluding DC.

Signal To Noise Ratio (SNR)

SNR is the ratio of the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components below $f_S/2$ excluding the fundamental, the first five harmonics and DC.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the fundamental input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the applicable harmonic component to the RMS value of the fundamental input signal.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spectral component in the spectrum below $f_S/2$.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f_1 and f_2, are present at the inputs. The ratio of the measured signal to the distortion terms is calculated. The terms included in the calculation are (f_1+f_2), (f_1-f_2), $(2f_1)$, $(2f_2)$, $(2f_1+f_2)$, $(2f_1-f_2)$, (f_1+2f_2), (f_1-2f_2). The ADC is tested with each tone 6dB below full scale.

Transient Response

Transient response is measured by providing a full-scale transition to the analog input of the ADC and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Over-Voltage Recovery

Over-Voltage Recovery is measured by providing a full-scale transition to the analog input of the ADC which overdrives the input by 200mV, and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Full Power Input Bandwidth (FPBW)

Full power input bandwidth is the analog input frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has an amplitude which swings from -FS to +FS. The bandwidth given is measured at the specified sampling frequency.

Video Definitions

Differential Gain and Differential Phase are two commonly found video specifications for characterizing the distortion of a chrominance signal as it is offset through the input voltage range of an ADC.

Differential Gain (DG)

Differential Gain is the peak difference in chrominance amplitude (in percent) relative to the reference burst.

Differential Phase (DP)

Differential Phase is the peak difference in chrominance phase (in degrees) relative to the reference burst.

Timing Definitions

Refer to Figure 1 and Figure 2 for these definitions.

Aperture Delay (t_{AP})

Aperture delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

Aperture jitter is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Hold Time (t_H)

Data hold time is the time to where the previous data (N - 1) is no longer valid.

Data Output Delay Time (t_{OD})

Data output delay time is the time to where the new data (N) is valid.

Data Latency (t_{LAT})

After the analog sample is taken, the digital data representing an analog input sample is output to the digital data bus on the 7th cycle of the clock after the analog sample is taken. This is due to the pipeline nature of the converter where the analog sample has to ripple through the internal subconverter stages. This delay is specified as the data latency. After the data latency time, the digital data representing each succeeding analog sample is output during the following clock cycle. The digital data lags the analog input sample by 7 sample clock cycles.

Power-Up Initialization

This time is defined as the maximum number of clock cycles that are required to initialize the converter at power-up. The requirement arises from the need to initialize the dynamic circuits within the converter.